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Modeling the Duration of the High Breakdown Voltage Phase in Deep Depletion Power Devices

Ettore NAPOLI

Dept. of Electronics and Telecommunication Engineering,
University of Napoli *Federico II*, Italy
E-mail: ettore.napoli@unina.it

Abstract. The paper presents a one dimensional model for the duration of the increased breakdown voltage phase in Deep Depletion power devices. The model includes the effect of bulk generation and space charge generation that is verified against numerical simulations of a nSi-BOX-pSi structure. The final result of the model, the duration of the high breakdown voltage phase as a function of device characteristic and the applied voltage, is verified against experimental results regarding the duration of the increased breakdown voltage phase in a power LDMOS in SOI technology. The results show that the interface states are probably the limiting factor for the duration of the increased breakdown voltage phase.

Key words: Deep Depletion, Lateral power MOS, carrier lifetime, silicon on insulator (SOI) technology.

1. Introduction

The research of improved power devices is of great importance due to the role of the power devices in the realization of power management circuits with higher efficiency reduced size and reduced cost.

A particular attention has been recently directed to the realization of Smart Power IC's whose target is the integration on a single chip of the power devices and of the control logic [1].

One of the most promising technologies is the Silicon On Insulator (SOI) that provides very good isolation between adjacent devices [1], [2]. Unfortunately the

SOI power devices suffer of a reduced Breakdown Voltage (BV) if compared with other techniques such as the junction isolation, since the substrate of the device is not depleted in the OFF state and hence does not contribute to sustain the drain voltage [1], [2]. The scientific literature presents a number of contributions that tend to improve the blocking properties of SOI based power devices. A review of the proposed techniques can be found in [3].

An innovative technique for the design of SOI power devices has been proposed in [3]–[8]. It uses the Deep Depletion (DD) of the SOI structure to obtain a transient modification of the electric field distribution in the device. The result is that, for a time interval that depends on silicon characteristics and temperature, the device exhibits a Transient BV (TrBV) higher than the static BV.

In [4] experimental results demonstrate the increased TrBV effect. In [5] a DD device is simulated in a complete switching topology, a resonant Class E converter, that is one of the most promising applications for DD devices. In [6] the DD concept is exploited in a new structure of Lateral Power MOS (LDMOS) with a selective doping of the substrate. In [7] an estimate of the duration of the TrBV is obtained through numerical simulations while in [8] the duration of the TrBV phase is experimentally measured.

This paper is based on the paper [9] presented at the 2007 International Semiconductor Conference, in Sinaia (RO) and proposes a one dimensional (1D) model of the DD effect in section 2. The model is compared with experimental results in section 3 while section 4 presents the model for the duration of the high breakdown voltage phase.

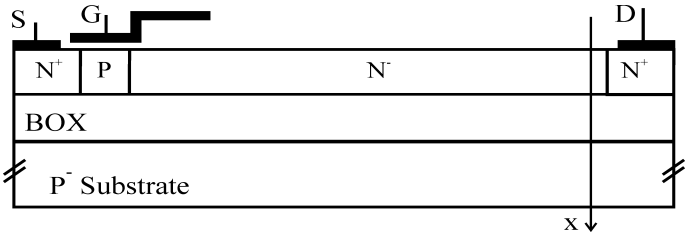

Fig. 1. Schematic section of the Deep Depletion LDMOS considered in the paper. The device is manufactured in Thin SOI technology with lightly doped substrate. The x axis shown on the right is the section considered in the derivation of the 1D model.

2. One dimensional model for Deep Depletion

The device considered in this paper is a Deep Depletion LDMOS whose schematic is shown in Fig. 1. The LDMOS is manufactured in Thin SOI technology with lightly doped substrate. The considered vertical 1D section, highlighted in Fig. 1, is a nSi-BOX-pSi structure. The nSi is a thin epilayer that corresponds to the active layer of the power device. The pSi is a thick layer that corresponds to the substrate of the SOI device. The net charge concentration corresponding to the considered section is shown in Fig. 2. The situation analyzed in this paper corresponds to the application

of a positive voltage at $x = 0$ while the other side of the structure ($x \gg W$) is grounded. In Fig. 2 the thickness of the various layers together with the thickness of the depleted region in the substrate (W) are indicated. The y axis in Fig. 2 indicates the net charge. The charge of the nSi layer is positive while the charge of the pSi is negative. The proposed model includes the effect of the inversion layer at the BOX-pSi interface indicated as $-Q_S$ (in this way Q_S is a positive value) in Fig. 2. The presence of an inversion layer at the nSi-BOX interface is neglected in this paper.

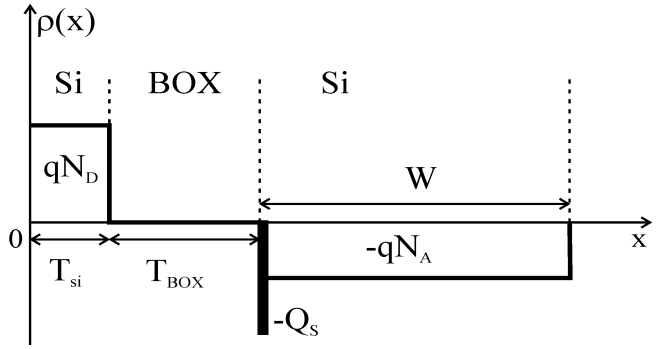

Fig. 2. Charge concentration in the considered nSi-BOX-pSi structure.
The charge profile corresponds to the vertical section highlighted in Fig. 1.

Depletion width: The depletion, W, can be calculated solving the one dimensional Poisson equation in the domain of Fig. 2. The assumption is that the nSi is completely depleted, a reasonable assumption due to the reduced thickness of the nSi layer. With this hypothesis the electric field is similar to what is shown in Fig. 3.

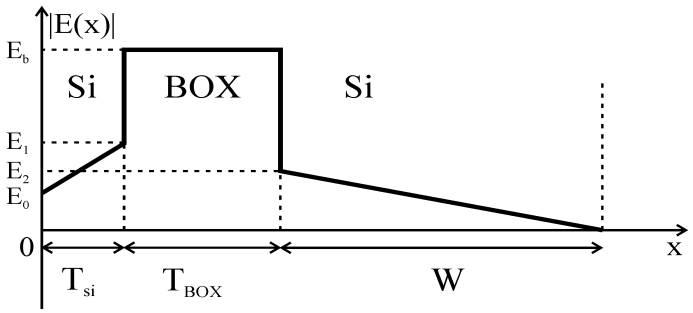

Fig. 3. Electric field in the considered nSi-BOX-pSi structure when
a positive voltage is applied at $x = 0$ and the nSi region is completely depleted.

The equations for the electric field in each layer and in particular points (E_0, E_1, E_2) indicated in Fig. 3, are:

$$\begin{cases} x = 0 \\ E\,(0) \triangleq E_0 \end{cases}, \tag{1}$$

$$\begin{cases} 0 < x < T_{si} \\ E(x) = E_0 + \dfrac{qN_D}{\varepsilon_s} x \end{cases}, \tag{2}$$

$$\begin{cases} x = T_{si} \\ E(T_{si}) = E_0 + \dfrac{qN_D}{\varepsilon_s} T_{si} \triangleq E_1 \end{cases}, \tag{3}$$

$$\begin{cases} T_{si} < x < T_{si} + T_{BOX} \\ E(x) = \left(E_0 + \dfrac{qN_D}{\varepsilon_s} T_{si} \right) \dfrac{\varepsilon_s}{\varepsilon_{ox}} = E_1 \dfrac{\varepsilon_s}{\varepsilon_{ox}} \end{cases}, \tag{4}$$

$$\begin{cases} x = T_{si} + T_{BOX} \\ E(T_{si} + T_{BOX}) = E_1 - \dfrac{Q_S}{\varepsilon_s} \triangleq E_2 \end{cases}, \tag{5}$$

$$\begin{cases} x > T_{si} + T_{BOX} \\ E(x) = E_2 - \dfrac{qN_A}{\varepsilon_s} (x - T_{si} - T_{BOX}) \end{cases}. \tag{6}$$

The depletion width, W, is the abscissa that corresponds to zero electric field in eq. (6), and is given by:

$$W = \frac{E_2 \varepsilon_s}{qN_A}. \tag{7}$$

The integration of the electric field over nSi, BOX and depleted pSi substrate is equal to the applied voltage, indicated as V_A:

$$V_A = E_1 T_{si} - \frac{qN_D}{\varepsilon_s} \frac{T_{si}}{2} + E_1 T_{BOX} \frac{\varepsilon_s}{\varepsilon_{ox}} + \frac{\varepsilon_s}{2qN_A} \left(E_1^2 + \frac{Q_S^2}{\varepsilon_s^2} - 2 \frac{Q_S}{\varepsilon_s} E_1 \right). \tag{8}$$

It is therefore possible to solve eq. (8) for E_1. With the positions:

$$X = 1 - \frac{2Q_S}{qN_A T_{eq}} + \frac{N_D T_{si}^2}{N_A T_{eq}^2} + \frac{2V_A \varepsilon_s}{qN_A T_{eq}^2}, \tag{9}$$

$$T_{eq} = T_{si} + T_{BOX} \frac{\varepsilon_s}{\varepsilon_{ox}}, \tag{10}$$

the result for E_1 is:

$$E_1 = \frac{Q_S}{\varepsilon_s} - \frac{qN_A T_{eq}}{\varepsilon_s} \left(\sqrt{X} - 1 \right). \tag{11}$$

E_1 is an important physical quantity since it is the peak electric field in the nSi layer and hence from E_1 it is possible to devise the presence or the absence of the breakdown condition.

W is obtained using (5) and (7). The result is:

$$W = T_{eq} \left(\sqrt{X} - 1 \right). \tag{12}$$

The first result that can be devised by the proposed model is the depletion width immediately after a fast voltage rise that forces the nSi-BOX-pSi structure in the DD regime. Since the voltage rise is fast with respect to the minority carriers generation time in the substrate, there is no time to generate an inversion layer and the initial depletion width is obtained fixing $Q_S = 0$ in eq. (12). The resulting depletion width at the beginning of the DD phase, W^0_{DD}, is:

$$W^0_{DD} = T_{eq}\left(\sqrt{1 + \frac{N_D T^2_{si}}{N_A T^2_{eq}} + \frac{2V_A\varepsilon_s}{qN_A T^2_{eq}}} - 1\right). \tag{13}$$

Note that the depletion width, when N_A is lower that N_D, can be much larger than the static depletion width in the substrate in static conditions. As a matter of fact the static width is obtained when the inversion layer is formed below the BOX and it is well known from the literature that such width is in the order of 1 µm.

It is also important to comment eq. (11) and eq. (3) that support the DD theory stating that, as a minority layer of charge builds up below the BOX ($Q_S > 0$), E_1 and E_0 increase. Consequently, when $Q_S = 0$ the measured BV is higher than the static BV.

Duration of the DD phase: During the DD phase the depletion width decreases due to the generation of minority carriers that populate the inversion layer and increase Q_S. The duration of the DD depletion phase is therefore directly influenced by the generation time of minority carriers. This effect has been studied by a number of authors that exploited the DD effect to characterize the silicon and the silicon oxide interface [10]–[14]. The experiments show that the contributions to the generation of the inversion layer are: the substrate space charge region (SCR) generation, J_g, characterized by the generation lifetime τ_g; quasi neutral bulk generation, J_b, characterized by the minority carriers diffusion length L_n, and the generation through the interface states. The contribution due to the interface states is neglected in this paper. The equations for these contributions are:

$$J_g = \frac{qn_i W_{DD}}{\tau_g}, \tag{14}$$

$$J_b = \frac{qn_i^2 D_n}{N_A L_n}. \tag{15}$$

Current described by eq. (15) can be considered constant during the DD transient, while current described by eq. (14) is proportional to W_{DD} that is a function of Q_S and hence is a function of the time. Using a first order Taylor expansion of (7) as a function of Q_S we have:

$$W_{DD}(Q_S) = W^0_{DD} - \frac{Q_S}{qN_A\left(W^0_{DD}/T_{eq} + 1\right)}. \tag{16}$$

The evolution of Q_S is determined by:

$$\frac{\mathrm{d}Q_S}{\mathrm{d}t} = J_0 - \frac{Q_S}{\tau_{DD}}. \tag{17}$$

With the positions $J_0 = J_b + qn_iW_{DD}^0/\tau_g$ and $\tau_{DD} = \tau_g \left(W_{DD}^0/T_{eq} + 1\right) \dfrac{N_A}{n_i}$ the time evolution of Q_S is described by:

$$Q_S(t) = \tau_{DD} J_0 \left[1 - \exp\left(-t/\tau_{DD}\right)\right]. \tag{18}$$

The one dimensional model has been compared with the numerical simulation of a structure whose characteristics are $T_{si} = 0.25$ μm, $T_{BOX} = 2$ μm, $N_D = 5{\times}10^{15}$ cm^{-3}, $N_A = 1 \times 10^{14}$ cm^{-3}. The considered lifetime model is a single trap SRH model with the energy level of the trap at the midgap. Lifetime values, equal for both electron and holes are 10 μs, 1 μs and 0.1 μs.

Numerical results for the behavior of the depletion width after the application of a step voltage whose amplitude is 300 V are shown in Fig. 4. The results of the model, obtained substituting (18) in (16), are also shown in Fig. 4. The model is in reasonable qualitative agreement with the numerical simulations.

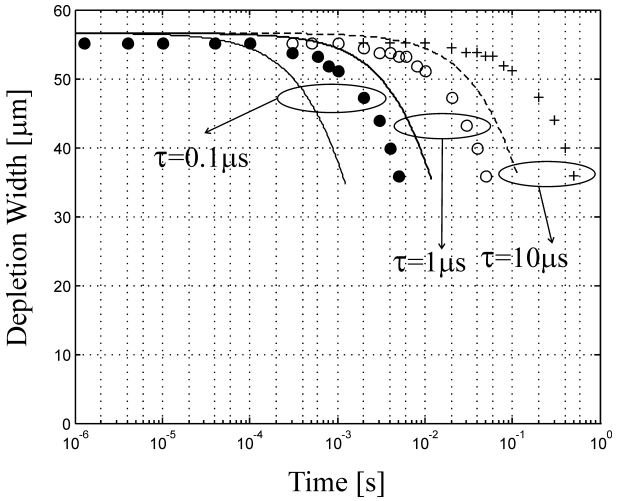

Fig. 4. Depletion width in the substrate as a function of time. Bullets, circles and crosses are the numerical results while thin line, thick line and dotted line are the results of the one dimensional model.

3. Experimental results

Experimental results regarding the duration of the TrBV phase have been obtained for a device similar to the one shown in Fig. 1. The device is a conventional LDMOS in thin SOI technology with 1 μm BOX. The substrate is lightly doped ($6{\times}10^{14}$ cm^{-3}) to enhance the DD effect. The static BV is 90V.

The duration of the increased breakdown voltage phase has been measured using a test circuit that applies the bus voltage to the Drain of the LDMOS for a predetermined period of time.

The experiment is conducted applying a voltage step at the Drain and measuring the leakage current. It has been considered that the device is able to sustain the given voltage if no leakage is measured on the oscilloscope.

The measures have been conducted for Drain voltages higher than the static BV. The duration of the pulse has been increased searching for the leaky condition that signals the end of the DD effect. The results are shown in Fig. 5.

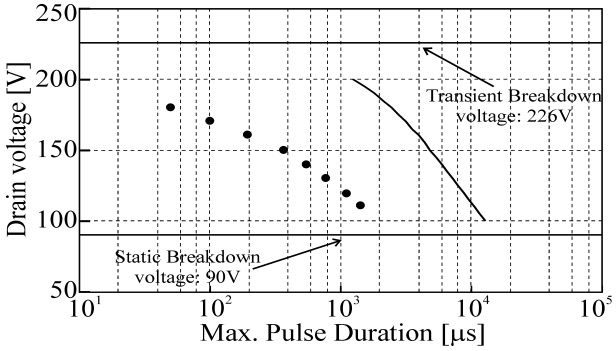

Fig. 5. Maximum duration of the Drain pulse vs. amplitude of the Drain pulse. Bullets: experimental results; solid line: model results.

The lower horizontal limit in Fig. 5 is the static breakdown voltage. The upper horizontal limit is the transient breakdown voltage value that corresponds to the Drain voltage that results in the instantaneous avalanche of the device. When the applied Drain voltage is between these two extremes a maximum duration of the pulse exists after which the breakdown arises and the device starts to leak.

The limit curve for the duration of the pulse as a function of the pulse amplitude is shown with bullets in Fig. 5. When the applied voltage is 110 V the pulse duration without measurable leakage is 1.5 ms. Increasing the drain voltage a reduction of the maximum pulse duration is observed. For a Drain voltage of 130 V,150 V and 170 V the measured maximum pulse duration are 0.8 ms, 380 μs and 100 μs, respectively. For the shortest pulse the TrBV has been measured as 226 V.

The results clearly demonstrate that the DD effect on the BV of a power device is a measurable effect whose duration is adequate for circuital applications.

4. Duration of the high breakdown voltage phase

Using the model of section 2 it is possible to give an estimate of the duration of the DD phase.

The first step is calculating the critical field E_1 that corresponds to the measured TrBV value. Using (5) and (7) the critical Q_S charge that brings E_1 to the value calculated above can be derived. Such critical charge is the charge that ceases the DD effect.

The results for the duration of the DD effect are shown in Fig. 5 with solid line. The model is able to predict a duration of the high breakdown voltage phase that

decreases with increasing applied voltage. The qualitative agreement between model and experiment is therefore good.

It is however visible a consistent quantitative disagreement between model and experiment in Fig. 5. This is a clue that the experiment is heavily affected by interface states that reduce the duration of the DD effect.

The inclusion of the effect of the interface states in the model will be addressed in a future work.

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